1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Non-PLL phase controlled Active EMI management architecture
- Generates a 1X low EMI Phase Modulated replication of the input signal.
- Vdd 1.65V - 3.6V. 10 MHz to 54 MHz
- Multiple Deviation Selections
- Minimum frequency deviation selection capability
- Power Down Mode
- 8-pin WDFN package
- Supports automotive reliability standard

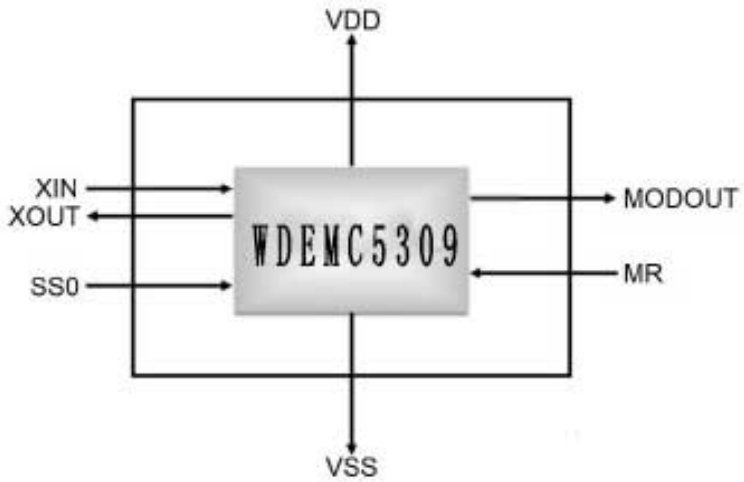
Product Description

The WDEMC5309 is a versatile 1x Active EMI management IC designed to provide system wide reduction of Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) from clock and data sources. The WDEMC5309 allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations. The WDEMC5309 family of mobile active EMI management ICs is unique in it's design and is based on PulseTake's phase controlled Active EMI management technology. This allows operation on aperiodic as well periodic signals.By the precise placement of the edges of the reconstructed input signal, the peak energy of the output is distributed over a wider and controlled energy band thereby significantly lowering system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators.
The WDEMC5309 has an input frequency range of 10MHZ to 54MHz over a wide voltage range of 1.65V to 3.6V.The device can be placed in a" non-modulated clock mode" by setting the SSEN pin to GND where sets the MODOUT pin to no modulated clock output.
The device has one "deviation control pins" SS0 to allow flexibility and optimization of both EMI compliance as well as in system design. The device is available in an 8 pin DFN package.

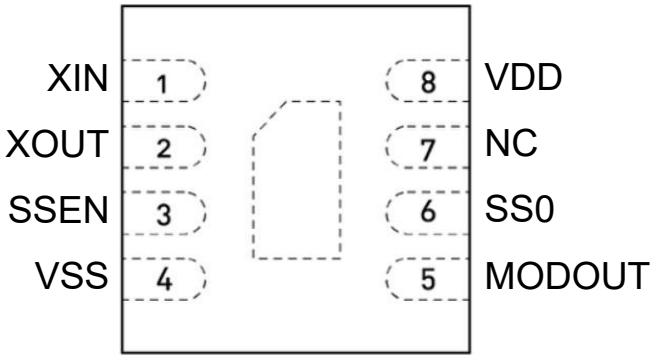
Applications

The WDEMC5309 is targeted towards mobile platforms such as cell phones, MIDs, Netbooks and other "power and space" sensitive applications.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Typ	Description
1	XIN	I	Crystal Oscillator Input
2	XOUT	O	Crystal Oscillator Output
3	SSEN	I	Modulated Clock Output if Pull-Up. No Modulated Clock Output if Pull-Down. Internal Pull-Up Resistor
4	VSS	P	System ground reference input.
5	MODOUT	O	1X phase modulated buffered output.
6	SS0	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Up Resistor. Recommend external Pull-Down Resistor 0Ω
7	NC	I	No Connection Pin
8	VDD	O	System Power Supply pin

Operating Conditions

Parameter	Description	Min	Max	Unit
$V_{DD(3.3V)}$	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+125	°C
C_L	Load Capacitance		20	pF
C_{IN}	Input Capacitance		5	pF

Note : Please refer to ordering information for T_A.

Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V_{in}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied nor guaranteed for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Functional Table

Device	Vdd	Freq. Range (MHz)	Freq. (MHz)	Deviation (%)	
				SS0	SS0
				0	1
WDEMC5309	1.8	10~40	12	±0.18	±0.28
	1.8		24	±0.35	±0.55
	1.8		27	±0.40	±0.60
	1.8		30	±0.36	±0.55
	3.3	10~54	12	±0.10	±0.15
	3.3		24	±0.20	±0.30
	3.3		27	±0.22	±0.34
	3.3		30	±0.21	±0.33

Note: Frequency deviation can vary over voltage and temperature by +/-20%.

DC Electrical Characteristics (3.3V +/-0.3V)

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			3.0	3.3	3.6	V
V_{IH}	Input HIGH Voltage			0.66*Vdd			V
V_{IL}	Input LOW Voltage					0.33*Vdd	V
I_{IH}	Input HIGH Current (pins 5 and 6)	$V_{IN} = V_{DD}$				10	µA
I_{IL}	Input LOW Current (pins 5 and 6)	$V_{IN} = 0V$				10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		0.75*Vdd			V
V_{OL}	Output LOW Voltage	I_{OL} = +8mA				0.25*Vdd	V
I_{CC}	Static Supply Current	PDB = VSS			0.1	1.0	µA
I_{DD}	Dynamic Supply Current (SS0=1)	27 MHZ	Unloaded		7.0	8	mA
			10 pF load		8.0	9	
Z_o	Output Impedance				25		Ω

Switching Characteristics (3.3V +/-0.3V)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		10	24	54	MHz
MODOUT	Output Frequency		10	24	54	
T_d	Duty Cycle [1,2] = (t_2 / t_1) * 100	Measured at V_{DD} /2	45	50	55	%
t_3	Output Rise Time [1,2]	Measured between 20% to 80%	0.6	1.5	2.5	nS
t_4	Output Fall Time [1,2]	Measured between 80% to 20%	0.6	1.4	2.5	nS
t_J	Cycle-to-cycle jitter [2]	Unloaded outputs 27 MHz		100		pS

Notes:
1.All parameters specified with loaded outputs.
2.Parameter is guaranteed by design and characterization. Not 100% tested in production.

DC Electrical Characteristics (1.8V +/-0.15V)

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			1.65	1.8	1.95	V
V_{IH}	Input HIGH Voltage			0.66*Vdd			V
V_{IL}	Input LOW Voltage					0.33*Vdd	V
I_{IH}	Input HIGH Current (pins 5 and 6)	V_{IN} = V_{DD}				10	µA
I_{IL}	Input LOW Current (pins 5 and 6)	V_{IN} = 0V				10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA		0.75*Vdd			V
V_{OL}	Output LOW Voltage	I_{OL} = +4mA				0.25*Vdd	V
I_{CC}	Static Supply Current	PDB = VSS			0.1	1.0	µA
I_{DD}	Dynamic Supply Current (SS0=1)	27 MHZ	Unloaded		3.0	4.0	mA
			10 pF load		3.5	4.5	
Z_o	Output Impedance				25		Ω

Switching Characteristics (1.8V +/-0.15V)

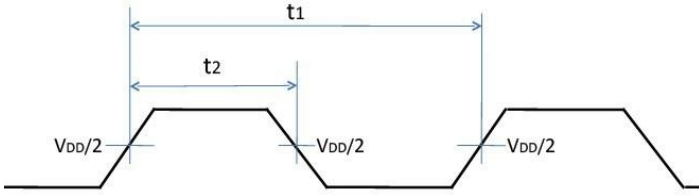
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		10	24	40	MHz
MODOUT	Output Frequency		10	24	40	
T_d	Duty Cycle [1,2] = (t_2 / t_1) * 100	Measured at V_{DD} /2	45	50	55	%
t_3	Output Rise Time [1,2]	Measured between 20% to 80%	0.8	1.5	1.8	nS
t_4	Output Fall Time [1,2]	Measured between 80% to 20%	0.8	1.0	1.8	nS
t_J	Cycle-to-cycle jitter [2]	Unloaded outputs 27 MHz		100		pS

Notes:

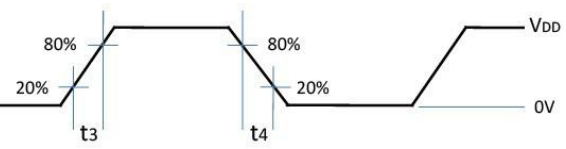
1 All parameters specified with loaded outputs.

2.Parameter is guaranteed by design and characterization. Not 100% tested in production.

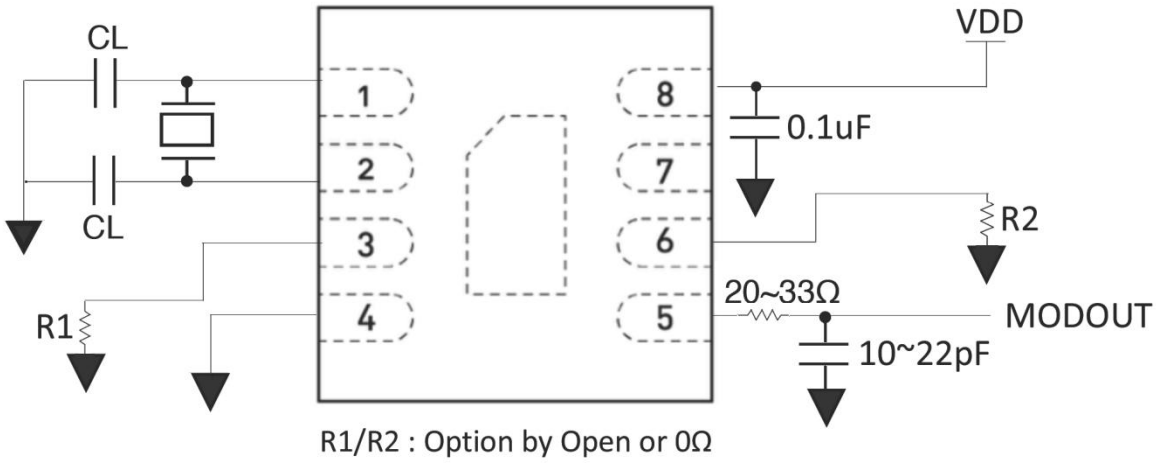
Duty Cycle Timing



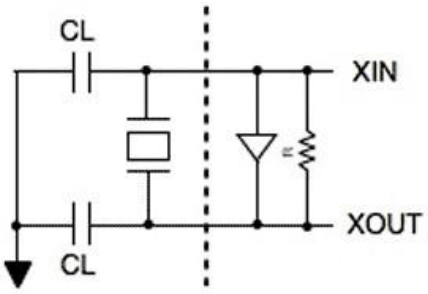
All Outputs Rise/Fall Time



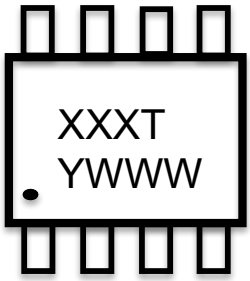
Application Schematic



R1/R2 : Option by Open or 0Ω



CL=2x(Cp-Cs)
Cp: load capacitance of Crystal
Cs: Stray capacitance (PCB trace + Input cap. of IC)

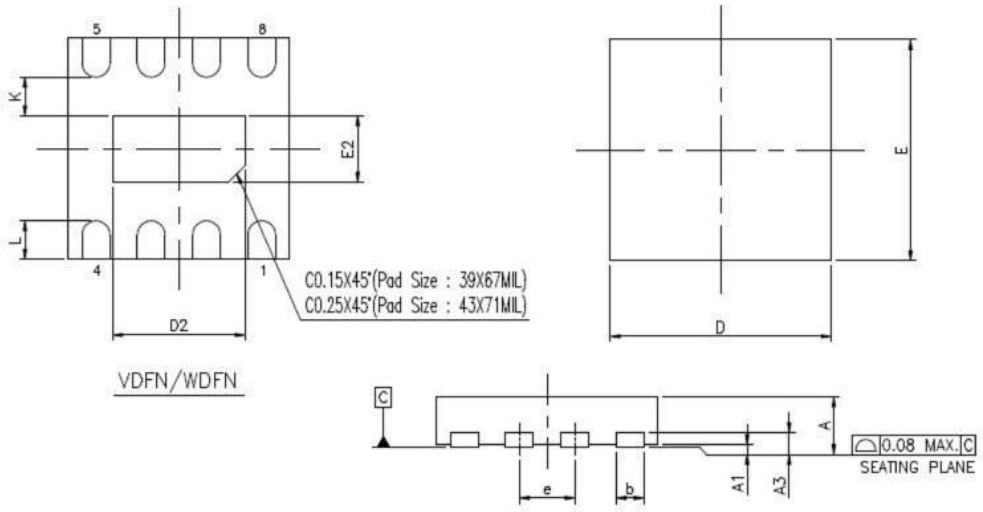


XXX: Part Code
T: Temperature Grade
Y: Year of Production
WWW: Work Order No.

Ordering Information

Part Number	Temp. Grade Indicator	Temp Grade	Temp Range	IC Marking	IC Package	Tape & Reel
WDEMC5309C	C	Commercial	0°~70°C	504C	2mm x 2mm 8L WDFN	4,000 pcs /Reel
WDEMC5309I	I	Industrial	-20°~85°C	504I		
WDEMC5309E	E	Automotive AEC Q100 Grade 2	-40°~105°C	504E		
WDEMC5309A	A	Automotive AEC Q100 Grade 1	-40°~125°C	504A		

Package Dimension
WDFN8 (X208)



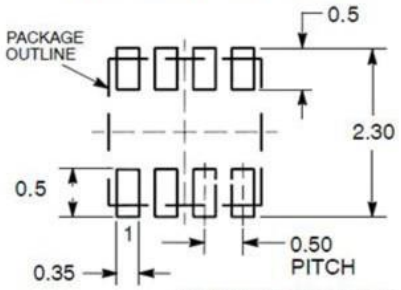
JEDEC OUTLINE	MO-229		
PKG CODE	WDFN (X208)		
SYMBOS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	.5 BSC		
K	0.20	---	---

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	D2			E2			L			LEAD FINISH		JEDEC CODE	VDFN	WDFN	UDFN	TDFN OPTION 1	TDFN OPTION 2
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
⚠ 39*X67* MIL	1.15	1.20	1.25	0.60	0.65	0.70	0.20	0.35	0.45	V	X	N/A	V	V			

⚠ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS